What is claimed is:

1. A differential detector for use in a digital frequency shift keying (FSK) receiver, comprising:

first means for receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal;

an arctan lookup table (LUT) for outputting a first phase value in accordance with each absolute scaled I signal and absolute scaled Q signal pair; and

second means for generating a delta phase value in accordance with said first phase value and a previous first phase value delayed one symbol time.

2. The detector according to claim 1, wherein said first phase value output by said arctan look up table is in the range of 0 to $\frac{\pi}{2}$.

3. The detector according to claim 1, further comprising a phase extractor operative to translate said first phase value output by said arctan lookup table in the range of 0 to $\frac{\pi}{2}$ to a second phase value in the range of $-\pi$ to $+\pi$ in accordance with the sign of said scaled I signal and said scaled Q signal.

4. The detector according to claim 1, wherein said scaled I signal and said scaled Q signal are generated by a baseband scaler module adapted to compress the bit representation of an input I signal and an input Q signal while maintaining their ratio of Q/I.

5. The detector according to claim 1, further comprising a clicks filter adapted to remove the discontinuity caused by said delta phase value wrapping around the $-\pi$ to $+\pi$ range.

6. The detector according to claim 1, wherein said arctan LUT comprises a 15 by 15 matrix of values.

7. The detector according to claim 1, further comprising means for reducing said arctan lookup table by a factor of approximately 2 utilizing the relationship arctan(x/y)=90°-arctan(y/x).

8. The detector according to claim 1, wherein frequency offsets within said scaled I signal and said scaled Q signal translate to DC offsets at the output of said arctan lookup table.

9. The detector according to claim 1, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

10. The detector according to claim 1, adapted to be implemented in a Field Programmable Gate Array (FPGA).

11. The detector according to claim 1, adapted to be implemented partially or entirely in software adapted to execute on an embedded microprocessor or digital signal processor.

12. A method of differential detection for use in a digital frequency shift keying (FSK) receiver, said method comprising the steps of:

receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal;

providing an arctan lookup table (LUT) adapted to output a preliminary phase value in the range of 0 to $\frac{\pi}{2}$ in accordance with each absolute scaled I signal and absolute scaled Q signal pair;

determining a resolved phase value in the range of $-\pi$ to $+\pi$ in accordance with the sign of said scaled I signal and said scaled Q signal; and

generating a delta phase value in accordance with said resolved phase value and a previous resolved phase value delayed one symbol time.

13. The method according to claim 12, wherein said scaled I signal and said scaled Q signal are scaled by compressing the bit representation of the input I signal and input Q signal while maintaining their ratio of Q/I.

14. The method according to claim 12 , further comprising the step of removing the discontinuity caused by said delta phase value wrapping around the $-\pi$ to $+\pi$ range.

15. The method according to claim 12, wherein said arctan LUT comprises a 15 by 15 matrix of values.

16. The method according to claim 12, further comprising the step of further reducing said arctan LUT by a factor of approximately 2 utilizing the trigonometric identity arctan(y/x)=90°-arctan(x/y).

17.   The method according to claim 12, wherein frequency offsets within said scaled I signal and said scaled Q signal translate to DC offsets at the output of said arctan lookup table.

18.   The method according to claim 12, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

19.   The method according to claim 12, adapted to be implemented in a Field Programmable Gate Array (FPGA).

20.   The method according to claim 12, adapted to be implemented partially or entirely in software adapted to execute on an embedded microprocessor or digital signal processor.

21.   A differential demodulator for use in a digital frequency shift keying (FSK) receiver, comprising:

    first means for receiving a scaled I signal and a scaled Q signal and determining the absolute value thereof to yield an absolute scaled I signal and an absolute scaled Q signal;

    second means for providing an arctan lookup table (LUT) adapted to output a first phase value in the range of 0 to $\frac{\pi}{2}$ in accordance with each absolute scaled I signal and absolute scaled Q signal pair;

    third means for determining a second phase value in the range of $-\pi$ to $+\pi$ in accordance with the sign of said scaled I signal and said scaled Q signal; and

    fourth means for generating a delta phase value in accordance with said second phase value and a previous second phase value delayed one symbol time.

22.   The demodulator according to claim 21, wherein said scaled I signal and said scaled Q signal are scaled by compressing the bit representation of an I signal and a Q signal while maintaining a ratio of Q/I.

23.   The demodulator according to claim 21, further comprising the step of removing the discontinuity caused by said delta phase value wrapping around the $-\pi$ to $+\pi$ range.

24.   The demodulator according to claim 21, wherein said arctan LUT comprises a 15 by 15 matrix of values.

25.   The demodulator according to claim 21, further comprising means for reducing said arctan lookup table by a factor of approximately 2 utilizing the relationship arctan(x/y)=90°-arctan(y/x).

26.   The demodulator according to claim 21, wherein frequency offsets within said scaled I signal and said scaled Q signal translate to DC offsets at the output of said arctan lookup table.

27.   The demodulator according to claim 21, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

28.   The demodulator according to claim 21, adapted to be implemented in a Field Programmable Gate Array (FPGA).

29.   The demodulator according to claim 21, adapted to be implemented partially or entirely in software adapted to execute on an embedded microprocessor or digital signal processor.